Application Bulletin AB-11

PC Board Layout Checklist: DC-DC Converters

Introduction

The design of switching power supplies presents unique design challenges due to its involvement with a variety of electrical, mechanical and magnetic components. In order to achieve a working design, care must be taken in the PC board layout, not just the electrical design. Due to the power involved in these circuits, component placement is critical for a robust and reliable design. The following presents a checklist of PC board design guidelines that should be followed in order to produce a working switching regulator design using Fairchild's RC50XX series of switchmode controllers.

Checklist

Item / Explanation	Yes / No
CAPACITOR PLACEMENT	
A 0.1μF capacitor is physically as close as possible to the V_{REF} pin . This helps ensure that the internal reference voltage is noise-free and stable.	
A 0.1μF capacitor is physically as close as possible to the V_{CCA} pin. This ensures that the +5V power running the internal logic of the IC is noise-free.	
A 1μF capacitor is physically as close as possible to the V_{CCP} pin. This capacitor provides bypass for the high currents used in driving the synchronous rectifier (lowside MOSFET).	
A 1μF capacitor is physically as close as possible to the V_{CCQP} pin. This capacitor provides bypass for the high currents used in driving the highside MOSFET.	
A 0.1μF capacitor is physically close to the drain pin of the highside MOSFET. This reduces the impedance presented by the input bulk capacitance at high switching speeds. If there is more than one highside MOSFET in parallel, each should have its own individual capacitor.	
The input bulk capacitance is physically located less than 1" from the drain of the power MOSFET(s). This reduces the impedance presented to the highside MOSFET.	
The output bulk capacitors are located physically as close to the CPU socket as possible. This minimizes the impedance seen by the CPU, optimizing transient performance.	
MOSFET PLACEMENT	
The controller IC and the power FET are oriented in such a way as to make the length of the gate drive trace < 1". This minimizes trace inductance, reducing gate ringing. If the trace is > 1", a 4.7Ω resistor must be used in series from the controller to the gate, one resistor for each MOSFET.	
The gate drive trace is routed on one layer only. This prevents gate noise from propagating to other layers.	
The gate drive trace routing stays away from the quiet analog sections of the RC50XX controller IC. (i.e., away from V_{REF}, IFB, VFB, and C_{EXT}.) This prevents gate noise from upsetting the analog functions of the controller.	
SENSE RESISTOR PLACEMENT	
The sense resistor is physically located close to the inductor. This minimizes the length of the power path, reducing losses.	

Checklist (continued)

Item / Explanation	Yes / No
The two traces that run from the sense resistor to the RC50XX controller IC are run parallel to each other, as close together as physically possible. This minimizes the noise pickup into the current limit.	
OTHER CONNECTIONS	
Each V_{CC} pin on the IC is connected to the 5V power plane through its own via. This helps prevent crosstalk.	
The controller IC receives its V_{CC} power from the system side of the input inductor and not the "dirty" side of the inductor (i.e., V_{CC} is NOT connected to the side that is connected to the power MOSFET drains). This keeps the switching noise from upsetting the analog functions of the controller.	
POWER PLANES	
High currents are located on planes, not traces. This minimizes losses.	
An internal power plane connects the source of the highside MOSFET, the inductor, and the flyback schottky diode (or the drain of the lowside MOSFET) together. This minimizes losses.	
GROUNDS	
All of the signal ground connections are attached together, and connect to the power ground plane at only one place, preferably the input capacitor ground. Separating signal and power ground avoids noise pickup into the analog functions of the controller.	
The controller IC has a continuous ground plane running underneath the entire chip area. This helps minimize noise pickup into the analog functions of the controller.	
Each of the IC's power ground pins has a separate via connection down into the ground plane. This minimizes ground bounce.	
Ground connections are short, and go directly to the ground plane. This minimizes ground bounce.	
Sensitive low-level signals are away from the active switching components. They use the ground plane as a shield. This helps minimize noise pickup into the analog functions of the controller.	

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